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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,057	12/04/2003	Hajime Kimura	12732-186001 / US6794	8774

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EXAMINER	
NGUYEN, KHAI M	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 08/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/727,057	KIMURA, HAJIME	
	Examiner	Art Unit	
	Khai M. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15,16,25,27,29,45 and 46* is/are allowed.

6)☒ Claim(s) *1-14,17-24,26,28 and 30-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-14, 17-24, 26, 28, and 30-44 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-14, 17-24, 26, 28, and 30-44 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakao (US 6,437,716) (hereinafter referred to as Nakao).

Regarding claims 1, Nakao discloses a semiconductor device (Fig. 4) comprising: a switching circuit (42) including: a plurality of input terminals (coupled to receive adjustment data from the data latch circuit 43 – see Fig. 1 and its associated text); a plurality of output terminals (selectively coupled to the terminal 48); and a plurality of current sources (8 current sources - 2, 2i, 4i, 8i, and 16i – of the upper and lower halves), wherein the current sources and the output terminals of the switching circuit (42) are electrically connected to each other (based on the data adjustment provided from 43), and the switching circuit (42) selects the output terminals to be connected to the input terminals by using signals which are input to the input terminals of the switching circuit (42), and a signal which is output from one of the output

terminals is inputted to one of the current sources for controlling or adjusting the current value flowing through the resister R (see Fig. 4 – column 9, lines 5-40).

Regarding claim 2, Nakao discloses the switching circuit (42) of claim 1 receiving a signal inputted externally (provided from the series resistor – Fig. 1).

Regarding claims 3-4, Nakao discloses a display device (LCD device – see the abstract and title) comprising the apparatus of claim 1.

Regarding claims 5, 9-10, Nakao discloses a display device (Fig. 4) comprising:

a switching circuit (42) including n-pieces of input terminals (coupled to receive inputs from 43), m-pieces of output terminals (selectively coupled to terminal 48), and m-pieces of current sources (i, 2i...),

wherein the current sources (I, 2i...) are each connected to one of the different output terminals (-2^J or $+2^J$, j = 1 to n),

at least one of the input terminals of the switching circuit (42) is connected to one or a plurality of switches (-2^J or $+2^J$, j = 1 to n),

the switch is connected to one of the m-pieces of the output terminals,

the switching circuit (42) controls ON/OFF of the switch by using a signal which is input from at least one of the n-pieces of the input terminals (coupled to 43), and

a signal which is output from at least one of the output terminals is input to at least one of the current sources for varying the output current provided to terminal 48 of Fig. 4.

Regarding claims 6, 22, 23, Nakao discloses a display device (Fig. 4) comprising:

a switching circuit (42) including a plurality of input terminals (coupled to receive inputs from 43) output terminals (selectively coupled to terminal 48), and current sources (i, 2i...),

wherein the current sources (I, 2i...) are each connected to one of the different output terminals (-2^J or $+2^J$, j = 1 to n),

at least one of the output terminals of the switching circuit (42) is connected to one or a plurality of switches (-2^J or $+2^J$, j = 1 to n),

the switch is connected to one of the input terminals,

the switching circuit (42) controls ON/OFF of the switch by using a signal which is input from at least one of the input terminals (coupled to 43), and

a signal which is output from at least one of the output terminals is input to at least one of the current sources for varying the output current provided to terminal 48 of Fig. 4.

Regarding claim 7, Nakao discloses the switching circuit (of claim 5) controls ON/OFF of the switching circuit by further using a signal, which is input externally (from the series resister – Fig. 1).

Regarding claim 8, Nakao discloses the switching circuit of 5 includes a digital circuit (43 – Fig. 4).

Regarding claim 11, Nakao discloses a DAC (see Fig. 4) comprising:

a switching circuit (42) including n-pieces of input terminals (coupled to receive inputs from 43), m-pieces of output terminals (coupled to terminal 48), and m-pieces of current sources (i, 2i...),

wherein the current sources (I, 2i...) are each connected to one of the different output terminals (-2^J or $+2^J$, j = 1 to n),

the switching circuit (42) selects one of the output terminals to be connected to at least one of the input terminals by using at least one of digital inputs (from the latch circuit 43 of Fig. 4), and

a signal which is output from at least one of the output terminals is input to at least one of the current sources for varying the output current provided to terminal 48 of Fig. 4.

Regarding claim 12, Nakao discloses the switching circuit (of claim 11) receiving a signal which is inputted externally (see Fig. 1 – from the series resister output the switching circuit 42).

Regarding claims 13, 28, Nakao discloses a display device comprising a DAC (Fig. 4), wherein the DAC includes:

a switching circuit (42) including n-pieces of input terminals (coupled to receive digital inputs from 43), m-pieces of output terminals (selectively coupled to terminal 48), m-pieces of switch units (as shown in Fig. 5, there are 10 switch units – 5 in the upper half and 5 in the lower half), and m-pieces of current sources (i, 2i...),

wherein the current sources (I, 2i...) are each connected to one of the different output terminals (-2^J or $+2^J$, j = 1 to n),

each of the switch units is connected to at least one input of the plurality of the input terminals,

the switching circuit (42) controls the switch units by using at least one of the digital signals inputted from the latch 43, thereby selecting an input terminal to be connected to the output terminal, and

a signal which is output from at least one of the output terminals is input to at least one of the current sources for varying the output current provided to terminal 48 of Fig. 4.

Regarding claim 14, Nakao discloses the switching circuit (of claim 11) receiving a signal, which is inputted externally (see Fig. 1 – from the series resister output the switching circuit 42).

Regarding claim 17, Nakao discloses the switching circuit of claim 11 includes a digital circuit (43 – Fig. 4).

Regarding claim 18, Nakao discloses a display device (LCD) comprising the DAC of claim 11 in a signal line driver circuit (Figs. 1, 4, 10-11).

Regarding claim 19, Nakao discloses an apparatus using its display portion a display device (LCD device – see the abstract and title) comprising the apparatus of claim 11.

Regarding claim 20, Nakao discloses the switching circuit (of claim 6) receiving a signal, which is inputted externally (see Fig. 1 – from the series resister output the switching circuit 42).

Regarding claim 21, Nakao discloses the switching circuit of 6 includes a digital circuit (43 – Fig. 4).

Regarding claim 24, Nakao discloses the switching circuit of 13 includes a digital circuit (43 – Fig. 4).

Regarding claim 26, Nakao discloses a display device (LCD) comprising the DAC of claim 13 in a signal line driver circuit (Figs. 1, 4, 10-11).

Regarding claims 30-34, Nakao discloses (when the switches as shown in Fig. 4 are turned on) the current sources and the output terminals of the switch circuit are connected directly to each other (Fig. 4).

Regarding claims 35-44, Nakao discloses a display device of these claims (see Figs. 1, 4, 6, 7, 10 and associated text).

3. Regarding claims 15-16, 25, 27, 29, and 45-46 are allowed.

Contact Information

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khai M. Nguyen whose telephone number is 571-272-1809. The examiner can normally be reached on 9:00 - 5:30 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert (Bob) J. Pascal can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KN
August 1, 2005

PEGUY JEANPIERRE
PRIMARY EXAMINER